REMARKS

This application has been carefully reviewed in light of the Advisory Action dated March 5, 2003. Claims 1, 16, and 31 have been amended. A marked-up version of these claims, showing changes made, is attached hereto as Appendix A. Claims 5, 17, and 19 have been canceled. Claims 1-3, 6-16, 18, 21-31, and 34-45 are pending in this application. Applicants request that the Examiner please reconsider the above-referenced application in light of the amendments and following remarks.

Claim 1 has been amended to positively recite that the second oxide layer is "grown by oxidizing said nitride layer with a gas ambient containing atomic oxygen, wherein said second oxide layer is formed to have a thickness of at least 60% of the targeted thickness of the second oxide layer." Support is found in Applicants' specification, pg. 12, lines 11-20. Applicants' specification further defines "targeted thickness" as any suitable and/or desired thickness for the top oxide layer 46c (Page 13, lines 1-3).

Similarly, claim 16 has been amended to positively recite that the second oxide layer is "grown at a temperature of about 850°C to about 1100°C, for about 1 second to about 10 minutes, using a gas ambient containing atomic oxygen." Support is found in Applicants' specification, pg. 12, lines 11-20.

Claim 31 has been amended to positively recite that the second oxide layer is "grown in the presence of atomic oxygen at a temperature of less than about 900°C." Support is found in Applicants' specification, pg. 12, lines 11-20.

Claims 1-6, 11-21, 26-31, 33-36, and 41-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang. Reconsideration is respectfully requested.

The Advisory Action states that "there is no basis for applicant's statement that the 'targeted' thickness in Wang is 50 Angstroms." (Advisory Action, pg. 2). Applicants respectfully disagree.

Wang teaches that the "second of the two oxide layers [e.g., the top oxide layer] . . . is formed using a nitride oxidation technique at about 950°C, with about 5 liters of O_2, and 9 liters of H_2 for about 40 minutes, which grows approximately 50 Å of oxide." (Col. 3, lines 49-54). Wang's resulting ONO structure is only 135 Å thick (Col. 3, line 54). Wang teaches that the first oxide layer is 50 Å thick and the nitride layer is 80 Å thick. Thus, the first two layers of Wang's ONO structure is 130 Å thick.

However, Wang's second oxide layer, although targeted to be 50 Å thick, results in only a 5 Å thick layer since the total thickness of the ONO structure is 135 Å thick. If the second oxide layer e.g., Wang's top oxide layer, does not have a "targeted" thickness of 50 Å, then Wang's resulting ONO structure would be 180 Å thick rather than 135 Å thick. Accordingly, Wang merely teaches a conventionally-formed ONO structure.

Applicants' claimed invention is directed toward fabricating a top oxide layer in an ONO structure with an actual thickness of at least about 60% of the targeted thickness. Conventionally formed top oxide layers, such as Wang's top oxide layer, resulted in a layer only 1-3% of the targeted thickness and required long periods of time for formation (Applicants' specification, pgs. 6-7 and 13).

Applicants' novel method allows formation of a top oxide layer that is actually 60% of a targeted value (Applicants' specification, pgs. 12-13). For instance, if the targeted thickness is 80 Å thick, the resulting top oxide layer would be at least 48 Å thick. Thus, applicants' resulting ONO structure is 178 Å thick, e.g., a first oxide layer 50 Å thick, a nitride layer 80 Å thick, and a second oxide layer 48 Å thick (Applicants' specification, pgs. 12-13). This resulting ONO structure is not possible utilizing the methods of taught in Wang.

To achieve this end, Applicants disclose a top oxide layer 46c grown under specific process conditions. For instance, as recited in claim 16, a top oxide layer is "grown at a temperature of about 850°C to about 1100°C . . . for about 1 second to about 10

minutes, using a gas ambient containing atomic oxygen." (Applicants' specification, pg. 12) (emphasis added). Wang does not teach or suggest these process parameters.

Further, Wang teaches depositing the layers of the ONO structure. Specifically, depositing the top oxide layer for a period of about 40 minutes and a temperature of 950°C. Wang does not teach or suggest a "grown" second oxide layer. Wang does not teach or suggest a second oxide layer that is grown from about 1 second to about 10 minutes. Wang teaches a top oxide layer that is deposited for a period of about 40 minutes. There is simply no teaching or suggestion in Wang to use Applicants' specific process conditions. In fact, Wang teaches nitride oxidation which is completely different from Applicants' oxidation process using atomic oxygen.

Further, the idea of providing a thicker ONO structure is contrary to the problem that Wang is trying to solve. Specifically, Wang teaches a method for reducing the gate aspect ratio of a flash memory device. A thicker ONO structure would increase the gate aspect ratio of a flash memory device rather than decrease it. If Wang's top oxide layer is actually 50 Å thick rather than being a targeted thickness as Applicants submit, then the total thickness of Wang's ONO structure would be 180 Å thick rather than 135 Å thick. Moreover, this would increase the gate aspect ratio of a flash memory device.

Accordingly, Wang does not teach or suggest that the "second oxide layer is grown by oxidizing said nitride layer with a gas ambient containing atomic oxygen, wherein said second oxide layer is formed to have a thickness of at least 60% of the targeted thickness of the second oxide layer," as claim 1 recites, nor a "second oxide layer [that] is grown at a temperature of about 850°C to about 1100°C, for about 1 second to about 10 minutes, using a gas ambient containing atomic oxygen," as claim 16 recites, or a "second oxide layer [that] is grown in the presence of atomic oxygen at a temperature of less than about 900°C," as claim 31 recites.

Claims 2-4, 6, and 11-15 depend from and incorporate all of the limitations found in independent claim 1, claims 18, 20-21, and 26-30 depend from and incorporate all of the limitations found in independent claim 16, and claims 33-36 and 41-45 depend from and incorporate all of the limitations found in independent claim 31. These claims are at least allowable for the reasons set forth above regarding independent claims 1, 16, and 31.

Therefore, the rejection for claims 1-3, 6, 11-16, 18, 21, 26-31, 34-36, and 41-45 should be withdrawn.

Claims 7-10, 22-25, and 37-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Neely. Reconsideration is respectfully requested.

Claims 7-10 depend from and incorporate all of the limitations found in independent claim 1, claims 22-25 depend from and incorporate all of the limitations found in independent claim 16, and claims 37-40 depend from and incorporate all of the limitations found in independent claim 31. These claims are at least allowable for the reasons set forth above regarding independent claims 1, 16, and 31 in view of Wang.

Neely is relied upon for another feature and adds nothing to rectify the deficiencies found in Wang. Neely is relied upon for teaching decomposing ozone under the presence of microwaves in order to promote oxidation. The Office Action asserts that it would be obvious to form the second oxide layer in Wang using the process taught by Neely to reduce the thermal budget of the oxidation in Wang. Applicants emphatically disagree.

Applicants are not arguing that the Wang reference relates to the formation of a control gate and that the Neely reference teaches forming an oxide layer, and therefore the references are not properly combinable. Rather, Applicants submit that Neely teaches an oxide layer formed under completely different process conditions than Wang's top oxide

layer. Further, there is no teaching or suggestion in Wang that a low thermal budget oxidation process is desired. In fact, Applicants submit that Wang teaches away from a low thermal budget oxidation process.

All of Wang's processes are conducted at high temperatures, e.g., at least greater than about 600°C. In fact, Wang requires "an anneal . . . performed on the nickel film at about 600°C, which causes the nickel film to react with the second polysilicon layer 412, forming a layer of nickel silicide 414." (Col. 4, lines 3-5).

In contrast, Neely teaches that high temperatures such as those "greater than 600° – 700° C.," resulted in imperfect silica films (Col. 2, lines 25-35). Wang requires a temperature of at least 600°C to react the nickel film with the second polysilicon layer 412. As a result, a lower gate aspect ratio is achieved in Wang. Accordingly, Wang teaches away from a low thermal budget process since a high temperature is required.

Further, Wang teaches that the top oxide layer is deposited at a temperature of about 950°C. Neely teaches not to use temperature greater than 600°C. The teachings of the references are inherently non-combinable. These arguments provide additional reasons for the allowance of claims 7-10, 22-25, and 37-40 in addition to those set forth above regarding independent claims 1, 16, and 31. Therefore, the rejection for claims 7-10, 22-25, and 37-40 should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicants

APPENDIX A

1. (Twice amended) A method of forming a flash memory cell, comprising:

forming a tunnel oxide on a substrate;

forming a first conductor layer over said tunnel oxide;

forming an insulating layer over said first conductor layer, said insulating layer comprising a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer, [wherein] said second oxide layer [is formed] grown by oxidizing said nitride layer with [an] a gas ambient containing atomic oxygen [for about 1 second to about 10 minutes], wherein said second oxide layer is formed to have a thickness of at least 60% of the targeted thickness of the second oxide layer;

forming a second conductor layer over said insulating layer;

etching at least said first conductor layer, said second conductor layer and said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in said substrate on an opposite side of said stacked gate structure, thereby forming at least one memory cell.

16. (Twice amended) A method of forming an ONO insulating structure, comprising:

depositing a first oxide layer over an integrated circuit structure;

depositing a nitride layer over said first oxide layer; and

growing a second oxide layer over said nitride layer wherein said second oxide layer is [formed by oxidizing said nitride layer in the presence of atomic oxygen, and

wherein said second oxide layer is formed to at least 60% of a targeted thickness of said second oxide layer] grown at a temperature of about 850°C to about 1100°C, for about 1 second to about 10 minutes, using a gas ambient containing atomic oxygen.

31. (Twice amended) A method of forming a flash memory array containing a plurality of flash memory cells, each of said plurality of flash memory cells being formed by the acts of:

forming a tunnel oxide on a substrate;

forming a first conductor layer over said tunnel oxide;

forming an insulating layer over said first conductor layer, said insulating layer comprising a first oxide layer over said first conductor layer, a nitride layer over said first oxide layer, and a second oxide layer over said nitride layer, wherein said second oxide layer is [formed by oxidizing said nitride layer] grown in the presence of atomic oxygen at a temperature of less than about 900°C;

forming a second conductor layer over said insulating layer;

etching at least said first conductor layer, said second conductor layer and said insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in said substrate, thereby forming at least one memory cell.